4 ELECTRICAL SPECIFICATIONS

4.1 Introduction

This chapter describes the electrical interface of the Cyrix III processor and provides AC and DC specifications.

4.2 Electrical Ground

All voltage values in Electrical Specifications are measured with respect to Vss ground (GND pins) unless otherwise noted.

4.3 Power Supply Voltage Signalling

The Cyrix III CPU operates using one power supply voltage (Vcc) typically at 2.2 volts, as determined by the VID bus. Hard-wired within the CPU, the 5-pin VID bus signals its core voltage requirement to the motherboard regulator.

4.4 Power and Ground Connections

The Cyrix III CPU contains 370 pins including 86 power pins and 80 ground (GND) pins. The power pins are divided into 73 Vcc pins, eight VREF pins and one Vcc_CMOS pin. The Vcc supply core voltage, the VREF pins are use to establish reference voltage for GTL+ logic (see below) and the Vcc_CMOS pin supplies I/O voltage to a portion of the I/O interface.

4.4.1 Decoupling

Testing and operating the Cyrix III CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the Cyrix III CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins.

4.5 Gunning Transceiver Logic

Many of the I/O interface signals in the Cyrix III and Celeron processors use a variation of the Gunning Transceiver Logic (GTL+) to help eliminate ringing and signal degradations caused by the fast switching.

The GTL+ logic uses a reference level voltage to determine switch point between a logical one and zero. The reference level voltage (VREF) is split into eight individual sources for individual decoupling and appears on eight VREF[7-0] pins to eliminate significant cross coupling.

4.5.1 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to ground (GND). When unused, these inputs do not require connection to external pull-up or pull-down resistors.

Table 4-1. Pins Connected to Internal Pull-Up Resistors

SIGNAL	PIN NO.	RESISTOR
BSEL1	AK30	20-kΩ down
BSEL0	AJ33	20-kΩ pull-up
TCK	AL33	20-kΩ pull-up
TDI	AN35	20-kΩ pull-up
THER-MTRIP#	AH28	20-kΩ pull-up
TMS	AK32	20-kΩ pull-up
TRST#	AN33	20-kΩ pull-up
EXTRATPIN#	AD2	20-kΩ pull-up-

4.5.2 NC Connection and Reserved Pins

Pins in the Cyrix III processor that are functional in the Celeron are left disconnected in the Cyrix III processor and designated as NC pins. These pins can be used as needed by the motherboard designer.

Reserved (RESV) pins are used by Cyrix for factory testing or for future use. These pins should not be connected to any component on the motherboard. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.5.3 Absolute MaximumRatings

The following table lists absolute maximum ratings for the Cyrix III CPU processors. Stresses beyond those listed under Table 4-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under “Recommended Operating Conditions” Table 4-3 (Page 4-136) is possible. Exposure to conditions beyond Table 4-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 4-2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Operating Case Temperature	5	85	°C	
Storage Temperature	-40	85	°C	
Max VID pin current		5	ma	

Notes:

1. Operating voltage is the voltage to which the component id designed to operate.
2. This rating applies to Vcc, and any input (except noted below) to the processor.
3. Parameter applies to CMOS and JTAG bus signal groups only.

4.6 Recommended Operating Conditions

Table 4-3 presents the recommended operating conditions for the Cyrix III CPU device.

Table 4-3. Recommended Operating Conditions for CMOS Signals

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
T_C	Operating Case Temperature	0		70	°C	Power Applied
$V_{CC\ CORE}$	Core Supply Voltage (2.2 V)	2.1		2.3	V	
$V_{IL\ CMOS}$	CMOS Input Low Voltage	-0.3		0.7	V	
$V_{IH\ CMOS}$	CMOS Input High Voltage	1.7		2.625	V	
$I_{OL\ CMOS}$	Output Low Current	14			mA	

Table 4-4. Recommended Operating Conditions for GTL+ Signals

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
$V_{IL\ GTL+}$	GTL+ Input Low Voltage	-0.3		0.82	V	
$V_{IH\ GTL+}$	GTL+ Input High Voltage	1.22		V_{TT}	V	
$I_{OL\ GTL+}$	GTL+ Output Low Current	36		48	mA	
$V_{TT\ GTL+}$	GTL+ Bus Termination Voltage	1.365	1.5	1.635	V	
$B_{TT\ GTL+}$	GTL+ Bus Termination Resistance		56		Ohms	
$V_{REF\ GTL+}$	GTL+ Input Reference Voltage	2/3 V_{TT} –2%	2/3 V_{TT}	2/3 V_{TT} +2%	V	

4.7 Bus Signal Groups

The Cyrix III bus can be divided into four bus-signals groups. These groups are listed in Table 4-5 below.

Table 4-5. Bus Signal Groups

SIGNAL TYPE	PARAMETER
GTL Input	BPRI#, DEFER#, RESET#, RS[2:0]#, TRDY#
GTL Input/Output	A[31:3]#, ADS#, BNR#, D[63:0]#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, REQ[4:0]#
CMOS Input	A20M#, BSEL0, BSEL1, CLK,FLUSH#, IGNNE#, INIT#, INTR, NMI, PWRGOOD, SMI#, SLP#, STPCLK#
CMOS Output	FERR#
Continuous DC Level	CPUPRES#, VID[4:0]

4.8 DC Characteristics

Table 4-6. DC Characteristics for CMOS Signals (at Recommended Operating Conditions)

SYMBOL	PARAMETER	MAX	UNIT	NOTES
V_{OL}	Output Low Voltage	0.4	V	
V_{OH}	Output High Voltage	2.625	V	
I_L	Leakage Current	± 100	uA	
I_{LO}	Output Leakage Current	± 10	uA	

Table 4-7. DC Characteristics for GTL+ Signals (at Recommended Operating Conditions)

SYMBOL	PARAMETER	MAX	UNITS	NOTES
V_{OL}	Output Low Voltage	0.60	V	Measured into 25 ohm resistor to 1.5v
V_{OH}	Output High Voltage	V_{TT}	V	See bus termination table
I_L	Leakage Current	± 100	uA	
I_{LO}	Output Leakage Current	± 15	uA	

Table 4-8. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	ICC CORE MAX	UNITS	NOTES
I_{CC} Active I_{CC}			Notes 1, 2
333 MHz	9.15	A	
366 MHz	9.76		
400 MHz	10.40		
433 MHz	10.85		
450 MHz	11.20		
$I_{CC\ SG}$ Stop Grant I_{CC}			Notes 1, 2, 3
PR 433 (333 MHz)	1.05	A	
PR 466 (366 MHz)	1.10		
PR 500 (400 MHz)	1.15		
PR 533 (433 MHz)	1.20		
PR 533 (450 MHz)	1.25		
$I_{CC\ SM}$ Sleep Mode I_{CC}			
PR 433 (333 MHz)	0.87	A	Notes 1, 2, 4
PR 466 (366 MHz)	0.89		
PR 500 (400 MHz)	0.91		
PR 533 (433 MHz)	0.93		
PR 533 (450 MHz)	0.95		

Notes:
1. These values should be used for power supply design. Maximum I_{CC} is determined using the worst-case instruction sequences and functions at maximum Vcc.
2. Frequency (MHz) ratings refer to the internal clock frequency.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

Table 4-9. Power Dissipation

PARAMETER	POWER	UNITS	NOTES
P_{CC} Active Power Dissipation			Note 1
PR 433 (333 MHz)	20.1	W	
PR 466 (366 MHz)	21.5		
PR 500 (400 MHz)	22.9		
PR 533 (433 MHz)	23.9		
PR 533 (450 MHz)	24.6		
P_{SG} Stop Grant Power Dissipation			Notes 1, 2
PR 433 (333 MHz)	2.31	W	
PR 466 (366 MHz)	2.42		
PR 500 (400 MHz)	2.53		
PR 533 (433 MHz)	2.64		
PR 533 (450 MHz)	2.75		
P_{SM} Sleep Mode Power Dissipation			Notes 1, 3
PR 433 (333 MHz)	1.91	W	
PR 466 (366 MHz)	1.96		
PR 500 (400 MHz)	2.00		
PR 533 (433 MHz)	2.05		
PR 533 (450 MHz)	2.09		

Notes:
1. Systems must be designed to thermally dissipate the maximum active power dissipation. Maximum power is determined using the worst-case instruction sequences and functions at maximum V_{CC}.
2. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).

4.9 AC Characteristics

The preliminary AC characteristics for the system bus clock, BCLK, and the Cyrix III GTL and CMOS signals at different bus clock speeds are listed in the tables below.

Table 4-10. 66 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		66.67		MHz	
T1	BCLK Period		15.0		ns	
T2	BCLK Period Stability			± 300	ps	
T3	BCLK High Time	3.6			ns	
T4	BCLK Low Time	3.6			ns	
T5	BCLK Rise Time	0.34		1.40	ns	0.5v to 2.0v
T6	BCLK Fall Time	0.34		1.40	ns	2.0v to 0.5v

Table 4-11. 100 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		100.00		MHz	
T1	BCLK Period		10.0		ns	
T2	BCLK Period Stability			± 250	ps	
T3	BCLK High Time	2.4			ns	
T4	BCLK Low Time	2.4			ns	
T5	BCLK Rise Time	0.34		1.40	ns	
T6	BCLK Fall Time	0.34		1.40	ns	

Table 4-12. 133 MHz System Bus AC Characteristics

SYMBOL	PARAMETER	MIN	TYPICAL	MAX	UNIT	NOTES
BCLK	System Bus Frequency		133.00		MHz	
T1	BCLK Period		7.5		ns	
T2	BCLK Period Stability			± 200	ps	
T3	BCLK High Time	1.8			ns	
T4	BCLK Low Time	1.8			ns	
T5	BCLK Rise Time	0.34		1.40	ns	
T6	BCLK Fall Time	0.34		1.40	ns	

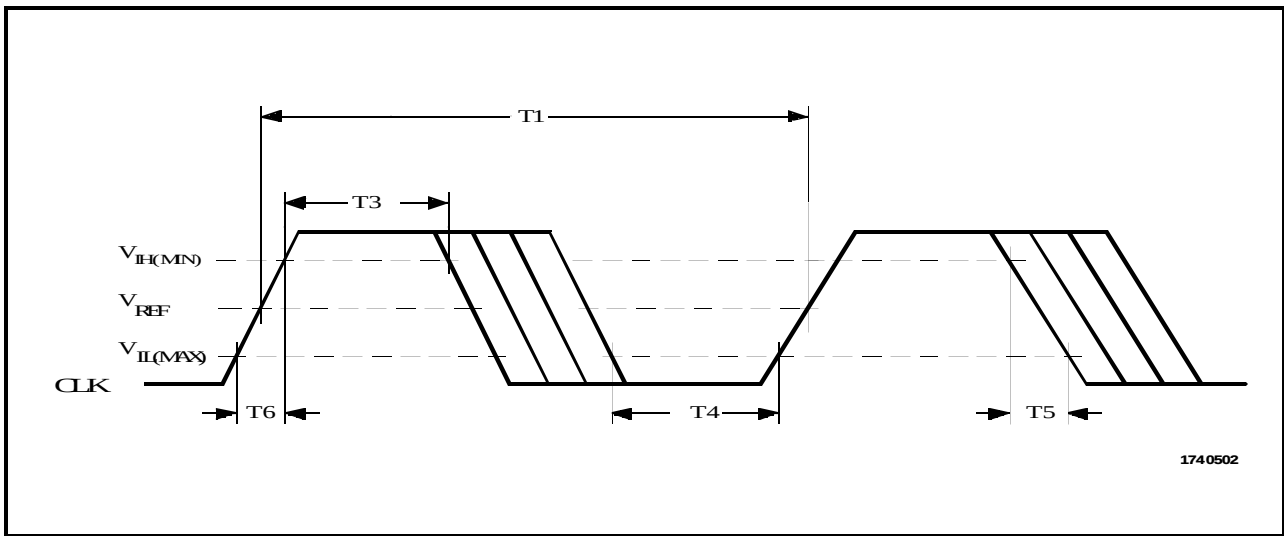

Figure 4-2. BCLK Timing and Measurement Points

Table 4-13. GTL+ Signal AC Characteristics

PARAMETER	66 MHz		100 MHz		133 MHz		UNIT	NOTES
	MIN	MAX	MIN	MAX	MIN	MAX		
GTL+ Output Valid Delay	0.17	4.40	0.17	3.45	0.17	3.00	ns	1,2
GTL+ Input Setup Time	1.60		1.60		1.40		ns	1
GTL+ Input Hold Time	0.90		0.90		0.90		ns	1
RESET Pulse Width	1.00		1.00		1.00		ms	3

Note:
1. All timings are referenced from the rising edge of BCLK at 1.25V and are measured to the GTL+ signal when it crosses 1.00 Volt.
2. Valid delay timings are specified for a 25 ohm resistance to V_{TT} and with V_{REF} at 1.0 Volt.
3. RESET# must remain asserted for the time specified after $V_{CC\ CORE}$ and BCLK are stable

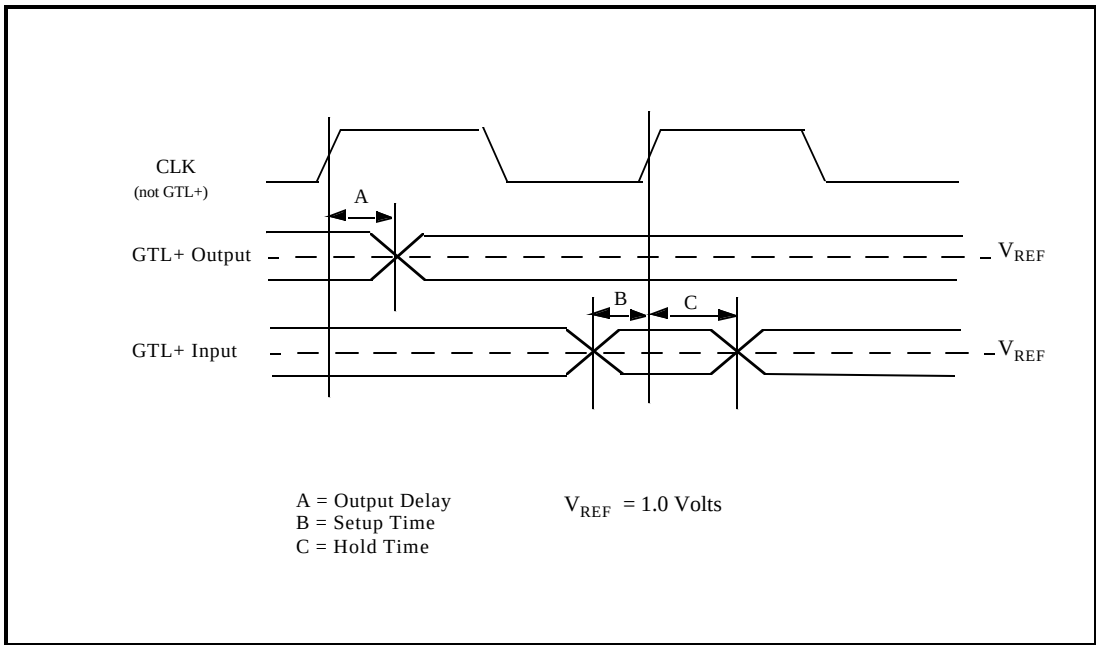

Figure 4-3. GTL+ Signal Definition

Table 4-14. CMOS Signal AC Characteristics

PARAMETER	66 MHz		100 MHz		133 MHz		UNIT	NOTES
	MIN	MAX	MIN	MAX	MIN	MAX		
2.5 V Output Valid Delay	0	8.0	0	8.0	0	7.0	ns	
2.5 V Input Setup Time	4.0		4.0		4.0		ns	See below
2.5 V Input Hold Time	1.3		1.3		1.3		ns	

Note. All timings are referenced from the rising edge of BCLK at 1.25V and are measured to the CMOS signal when it crosses 1.25 V.olts.

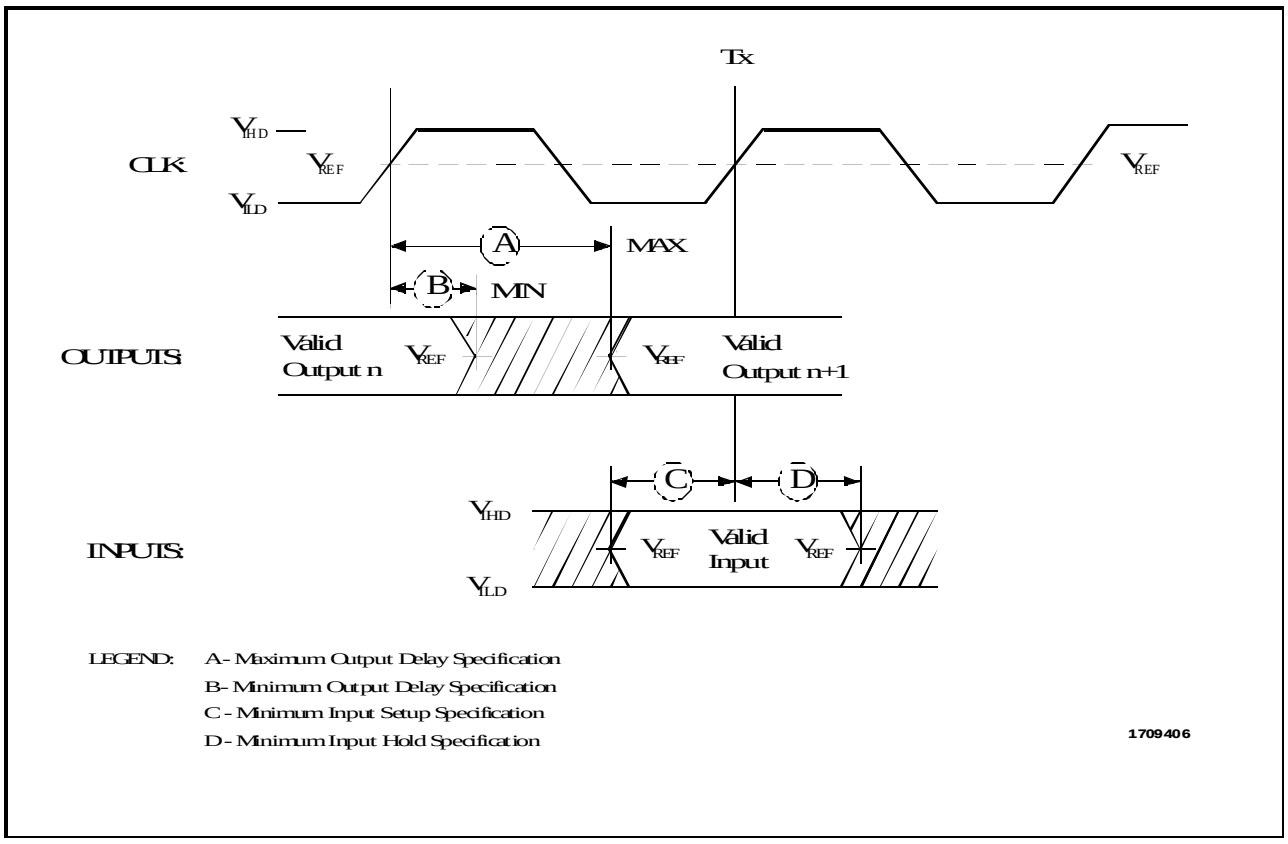

Figure 4-4. Drive Level and Measurement Points for Switching Characteristics